Notice of Allowability	Application No.	Applicant(s)	
	10/665,324	HASHIZUME ET AL.	
	Examiner	Art Unit	
	Dan I. Davidson	2627	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address--

All claims being allowable, PROSECUTION ON THE MERITS IS (OR REMAINS) CLOSED in this application. If not included herewith (or previously mailed), a Notice of Allowance (PTOL-85) or other appropriate communication will be mailed in due course. **THIS NOTICE OF ALLOWABILITY IS NOT A GRANT OF PATENT RIGHTS.** This application is subject to withdrawal from issue at the initiative of the Office or upon petition by the applicant. See 37 CFR 1.313 and MPEP 1308.

1. ☒ This communication is responsive to *September 30, 2006*.

2. ☒ The allowed claim(s) is/are *2-3, 5-6, 11-12, 15-16 renumberd as 2, 1, 4, 3, and 5-8*.

3. ☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).
   a) ☐ All b) ☐ Some* c) ☐ None of the:
      1. ☐ Certified copies of the priority documents have been received.
      2. ☐ Certified copies of the priority documents have been received in Application No. _____ .
      3. ☐ Copies of the certified copies of the priority documents have been received in this national stage application from the International Bureau (PCT Rule 17.2(a)).

   * Certified copies not received: _____.

Applicant has THREE MONTHS FROM THE "MAILING DATE" of this communication to file a reply complying with the requirements noted below. Failure to timely comply will result in ABANDONMENT of this application.
THIS THREE-MONTH PERIOD IS NOT EXTENDABLE.

4. ☐ A SUBSTITUTE OATH OR DECLARATION must be submitted. Note the attached EXAMINER'S AMENDMENT or NOTICE OF INFORMAL PATENT APPLICATION (PTO-152) which gives reason(s) why the oath or declaration is deficient.

5. ☐ CORRECTED DRAWINGS (as "replacement sheets") must be submitted.
   (a) ☐ including changes required by the Notice of Draftsperson's Patent Drawing Review (PTO-948) attached
      1) ☐ hereto or 2) ☐ to Paper No./Mail Date _____.
   (b) ☐ including changes required by the attached Examiner's Amendment / Comment or in the Office action of Paper No./Mail Date _____.

   Identifying indicia such as the application number (see 37 CFR 1.84(c)) should be written on the drawings in the front (not the back) of each sheet. Replacement sheet(s) should be labeled as such in the header according to 37 CFR 1.121(d).

6. ☐ DEPOSIT OF and/or INFORMATION about the deposit of BIOLOGICAL MATERIAL must be submitted. Note the attached Examiner's comment regarding REQUIREMENT FOR THE DEPOSIT OF BIOLOGICAL MATERIAL.

Attachment(s)

1. ☐ Notice of References Cited (PTO-892)
2. ☐ Notice of Draftperson's Patent Drawing Review (PTO-948)
3. ☐ Information Disclosure Statements (PTO/SB/08), Paper No./Mail Date _____
4. ☐ Examiner's Comment Regarding Requirement for Deposit of Biological Material
5. ☐ Notice of Informal Patent Application
6. ☐ Interview Summary (PTO-413), Paper No./Mail Date _____ .
7. ☒ Examiner's Amendment/Comment
8. ☐ Examiner's Statement of Reasons for Allowance
9. ☐ Other _____.

EXAMINER'S AMENDMENT

1. An examiner's amendment to the record appears below. Should the changes and/or additions be unacceptable to applicant, an amendment may be filed as provided by 37 CFR 1.312. To ensure consideration of such an amendment, it MUST be submitted no later than the payment of the issue fee.

Authorization for this examiner's amendment was given in a telephone interview with Mr. Carlton H. Hoel on October 11, 2006.

The application has been amended as follows beginning on the next page:

Amendments to the Specification:

The paragraph beginning at page 5, line 13 has been replaced with the following amended paragraph:

-- -- First drive unit 54 includes a high DC write (direct current) signal (WDHX1) source 60, a low DC write signal (WDLX1) source 62, a high boost signal (BSTHX1) source 64 and a low boost signal (BSTLX1) source 66. First drive unit 54 responds to control unit [68] 58 to selectively provide drive signals to a first connection locus 53 of write head 52. Second drive unit 56 includes a high DC write (direct current) signal (WDHX2) source 70, a low DC write signal (WDLX2) source 72, a high boost signal (BSTHX2) source 74 and a low boost signal (BSTLX2) source 76. Second drive unit 56 responds to control unit 58 to selectively provide drive signals to a second connection locus 55 of write head 52. -- --

The paragraph beginning at page 6, line 25 has been replaced with the following amended paragraph:

-- -- High boost signal source 64 is embodied in a primary current mirror component 150 operating with a secondary current mirror component 154 (a first boost current mirror). Low boost signal source 66 is embodied in primary current mirror component 150 operating with a secondary current mirror component 156 (a second boost current mirror). -- --

The paragraph beginning at page 7, line 1 has been replaced with the following amended paragraph:

-- -- Primary current mirror component 150 includes a diode-coupled transistor 160 in series with a transistor 162 between a signal input locus 165 and an upper voltage supply line 138 maintained substantially at an upper supply voltage V_{CC}. A boost

current reference signal I_{BSTREF} is applied at signal input locus 165. Boost signal I_{BSTREF} establishes the boost signal level for effecting data indications in write head 52. Current mirror component 150 further includes a diode connected transistor 164 coupled in series with transistors 166, 168 between lower voltage supply line 108 and upper voltage supply line 138 via a transistor 169. Preferably transistors 160, 164, 166 are bipolar transistors and transistors 162, 168, 169 are metal oxide silicon (MOS) transistors. Transistors 162, 168 are gated by bias signal V_{REF2}. Bias signal V_{REF1} gates transistor 169 so that boost signal I_{BSTREF} is permitted to flow through transistors 164, 166, 168, 169. Transistors 160, 162, 166, 168 cooperate to mirror boost signal I_{BSTREF} (biased toward upper voltage signal V_{CC}) to flow through transistors 170, 172 when transistor 172 is gated to conduct. Transistor 164 cooperates with transistors 160, 162, 166, 168 [cooperate] to mirror boost signal I_{BSTREF} (biased toward lower voltage signal V_{EE}) to flow through transistors 174, 176 when transistor 176 is gated to conduct. Transistor 176 is gated by control unit 58 in response to data signals 80 applying a gating signal BSTLX1 to gate locus 177 via network 68 (not shown in detail in FIG. 2) so that boost signal I_{BSTREF} (biased toward lower voltage signal V_{EE}) flows through transistors 174, 176 and is applied via junction 122 and network 78 to first connection locus 53 of write head 52. Transistor 172 is gated by control unit 58 in response to data signals 80 applying a gating signal BSTHX1 to gate locus 173 via network 68 (not shown in detail in FIG. 2) so that boost signal I_{BSTREF} (biased toward higher voltage signal V_{CC}) flows through transistors 170, 172 and is applied via junction 122 and network 78 to first connection locus 53 of write head 52. – –

The paragraph beginning at page 8, line 1 has been replaced with the following amended paragraph:

– – [Low] High DC write signal source 70 is embodied in a current mirror 200. Low DC write signal source 72 is embodied in a current mirror 202. Current mirror 202 includes a diode-coupled transistor 204 in series with a transistor 206 between a signal input locus 205 and a lower voltage supply line 208 maintained substantially at a lower

supply voltage V_{EE}. A direct current (DC) signal I_{WDC} is applied at signal input locus 205. Signal I_{WDC} establishes the direct current signal level for effecting data indications in write head 52. Current mirror 202 further includes transistors 210, 212 coupled in series between current mirror 200 and lower voltage supply line 208 and transistors 214, 216 coupled in series between current mirror 200 and lower voltage supply line 208. Preferably transistors 204, 210, 214 are bipolar transistors and transistors 206, 212, 216 are metal oxide silicon (MOS) transistors. A bias signal V_{REF1} gates transistors 206, 212 so that current signal I_{WDC} is permitted to flow through transistors 204, 206. That causes current signal I_{WDC} to be mirrored (biased toward lower voltage signal V_{EE}) in the circuit segment including transistors 210, 212. Transistor 216 is gated by control unit 58 in response to data signals 80 applying a gating signal WDLX2 to gate locus 217 via network 68 (not shown in detail in FIG. 2) so that current signal I_{WDC} (biased toward lower voltage signal V_{EE}) also is mirrored in the circuit segment including transistors 214, 216. When control unit 58 gates transistor 216 to conduct, current signal I_{WDC} (biased toward lower voltage signal V_{EE}) is applied via junctions 220, 222 and network 79 to second connection locus 55 of write head 52.

The paragraph beginning at page 9, line 6 has been replaced with the following amended paragraph:

High boost signal source 74 is embodied in a primary current mirror component 250 operating with a secondary current mirror component 252 (a first boost current mirror). Low boost signal source 76 is embodied in primary current mirror component 250 operating with a secondary current mirror component 256 (a second boost current mirror).

The paragraph beginning at page 9, line 9 has been replaced with the following amended paragraph:

-- Primary current mirror component 250 includes a diode-coupled transistor 260 in series with a transistor 262 between a signal input locus 265 and an upper voltage supply line 238 maintained substantially at an upper supply voltage V_{CC}. A boost current reference signal I_{BSTREF} is applied at signal input locus 265. Boost signal I_{BSTREF} establishes the boost signal level for effecting data indications in write head 52. Current mirror component 250 further includes a diode connected transistor 264 coupled in series with transistors 266, 268 between lower voltage supply line 208 and upper voltage supply line 238 via a transistor 269. Preferably transistors 260, 264, 266 are bipolar transistors and transistors 262, 268, 269 are metal oxide silicon (MOS) transistors. Transistors 262, 268 are gated by bias signal V_{REF2}. Bias signal V_{REF1} gates transistor 269 so that boost signal I_{BSTREF} is permitted to flow through transistors 264, 266, 268, 269. Transistors 260, 262, 266, 268 cooperate to mirror boost signal I_{BSTREF} (biased toward upper voltage signal V_{CC}) to flow through transistors 270, 272 when transistor 272 is gated to conduct. Transistor 264 cooperates with transistors 260, 262, 266, 268 [cooperate] to mirror boost signal I_{BSTREF} (biased toward lower voltage signal V_{EE}) to flow through transistors 274, 276 when transistor 276 is gated to conduct. Transistor 276 is gated by control unit 58 in response to data signals 80 applying a gating signal BSTLX2 to gate locus 277 via network 68 (not shown in detail in FIG. 2) so that boost signal I_{BSTREF} (biased toward lower voltage signal V_{EE}) flows through transistors 274, 276 and is applied via junction 222 and network 79 to second connection locus 55 of write head 52. Transistor 272 is gated by control unit 58 in response to data signals 80 applying a gating signal BSTHX2 to gate locus 273 via network 68 (not shown in detail in FIG. 2) so that boost signal I_{BSTREF} (biased toward higher voltage signal V_{CC}) flows through transistors 270, 272 and is applied via junction 222 and network 79 to second connection locus 55 of write head 52. --

The paragraph beginning at page 10, line 13 has been replaced with the following amended paragraph:

-- For example, if a data signal 80 is received by control unit 58 indicating a signal excursion in a direction that should be represented by a high write signal, then control unit 58 will gate transistor 136 and transistor 172 to effect application of a high DC write signal [(WDHX1)] and a high boost signal [BSTHX1)] at connection locus 53 of write head 52. At substantially the same time control unit 58 will gate transistor 216 and transistor 276 to effect application of a low DC write signal [(WDLX2)] and a low boost signal [BSTLX2)] at connection locus 55 of write head 52. Since DC signals and boost signals applied to connection loci 53, 55 are equal in magnitude and opposite in polarity, no pulse will be induced in adjacent read lines (not shown in FIG 2). --

The paragraph beginning at page 10, line 22 has been replaced with the following amended paragraph:

-- By way of further example, if a data signal 80 is received by control unit 58 indicating a signal excursion in a direction that should be represented by a low write signal, then control unit 58 will gate transistor 116 and transistor 176 to effect application of a low DC write signal [(WDLX1)] and a low boost signal [BSTLX1)] at connection locus 53 of write head 52. At substantially the same time control unit 58 will gate transistor 236 and transistor 272 to effect application of a high DC write signal [(WDHX2)] and a high boost signal [BSTHX2)] at connection locus 55 of write head 52. So long as DC signals and boost signals applied to connection loci 53, 55 are equal in magnitude and opposite in polarity, no pulse will be induced in adjacent read lines (not shown in FIG 2). --

Amendments to the Claims:

The listing of claims will replace all prior versions, and listings, of claims in the application:

Listing of claims:

Claim 1 (cancelled).

Claim 2 (currently amended): An apparatus for effecting symmetric driving of a write head as recited in claim 3 wherein said [at least one] first and second drive signals include[s] a direct current [write current] signal.

Claim 3 (currently amended): An apparatus for effecting symmetric driving of a write head[;], the apparatus comprising:

(a) a first drive unit coupled with a first connection locus of said write head;

(b) a second drive unit coupled with a second connection locus of said write head; and

(c) a control unit coupled with said first drive unit and said second drive unit;

said control unit effecting complementary coordination by said first and second drive units to provide a first drive signal from said first drive unit at said first connection locus and a second drive signal from said second drive unit at said second connection locus, said first and second drive signals in substantially equal magnitudes and of opposite polarities during respective time intervals of operation of said write head,

wherein said first drive unit comprises at least one first current mirror structure and said second drive unit comprises at least one second current mirror structure substantially similar to said at least one first current mirror structure, and wherein said [at least one] first and second drive signals include[s] a [write] boost [current] signal.

Claim 4 (cancelled).

Claim 5 (previously presented): An apparatus for effecting symmetric driving of a write head as recited in claim 3 wherein said respective time intervals of operation are intervals of a digital data signal.

Claim 6 (original): An apparatus for effecting symmetric driving of a write head as recited in claim 2 wherein said respective time intervals of operation are intervals of a digital data signal.

Claim 7 (cancelled).

Claim 8 (cancelled).

Claim 9 (cancelled).

Claim 10 (cancelled).

Claim 11 (currently amended): An apparatus for driving a write head in response to at least one data signal[;], the apparatus comprising:

(a) a first drive unit coupled with said write head;

(b) a second drive unit coupled with said write head; and

(c) a control unit coupled with said first drive unit and said second drive unit;

said control unit receiving said at least one data signal and generating control signals to said first drive unit and said second drive unit in response to said at least one data signal; said control signals controlling said first drive unit to apply at least one first drive signal to a first write head connection locus of said write head in a first signal polarity and controlling said second drive unit to apply at least one second drive signal to a second write head connection locus of said write head in a second signal polarity opposite to said first signal polarity when said at least one data signal effects a signal excursion; said at least one first drive signal and said at least one second drive signal

being substantially equal in magnitude; said at least one first drive signal and said at least one second drive signal being applied substantially simultaneously,

wherein each of said first drive unit and said second drive unit are substantially similar in construction and comprise: a first [secondary] boost current mirror and a second [secondary] boost current mirror; each of said first and second [secondary] boost current mirrors being coupled to receive a boost signal; each respective [secondary] boost current mirror of said first and second [secondary] boost current mirrors responding to said control signals to present a [write] boost [current] signal level to said write head [in the same signal polarity as said representative direct current write drive signal presented by said respective current mirror].

Claim 12 (currently amended): An apparatus for driving a write head in response to at least one data signal[;], the apparatus comprising:

(a) a first drive unit coupled with said write head;

(b) a second drive unit coupled with said write head; and

(c) a control unit coupled with said first drive unit and said second drive unit;

said control unit receiving said at least one data signal and generating control signals to said first drive unit and said second drive unit in response to said at least one data signal; said control signals controlling said first drive unit to apply at least one first drive signal to a first write head connection locus of said write head in a first signal polarity and controlling said second drive unit to apply at least one second drive signal to a second write head connection locus of said write head in a second signal polarity opposite to said first signal polarity when said at least one data signal effects a signal excursion; said at least one first drive signal and said at least one second drive signal being substantially equal in magnitude; said at least one first drive signal and said at least one second drive signal being applied substantially simultaneously,

wherein said each of said first drive unit and said second drive unit are substantially similar in construction and comprise: a first logic level current mirror and a second logic level current mirror; each of said first and second logic level current mirrors being coupled to receive a direct current signal and responding to said control signals to

present a [representative logic level write drive signal related to said] direct current signal level to said write head in one of said first signal polarity or said second signal polarity, and

wherein each of said first drive unit and said second drive unit [are substantially similar in construction and] comprise: a first [secondary] boost current mirror and a second [secondary] boost current mirror; each of said first and second [secondary] boost current mirrors being coupled to receive a boost signal; each respective [secondary] boost current mirror of said first and second [secondary] boost current mirrors responding to said control signals to present a [write] boost [current] signal level to said write head in the same signal polarity as said direct current signal level [representative logic level write drive signal presented by said respective current mirror].

Claim 13 (cancelled).

Claim 14 (cancelled).

Claim 15 (currently amended): A method for driving a write head in response to at least one data signal[;], the method comprising the steps of:

(a) in no particular order:

(1) providing a first drive unit coupled with said write head;

(2) providing a second drive unit coupled with said write head; and

(3) providing a control unit coupled with said first drive unit and said second drive unit; and

(b) operating said control unit to receive said at least one data signal and generate control signals to said first drive unit and said second drive unit in response to said at least one data signal; said control signals controlling said first drive unit to apply at least one first drive signal to a first write head connection locus of said write head in a first signal polarity and controlling said second drive unit to apply at least one second drive signal to a second write head connection locus of said write head in a second signal polarity opposite to said first signal polarity when said at least one data signal

effects a signal excursion; said at least one first drive signal and said at least one second drive signal being substantially equal in magnitude; said at least one first drive signal and said at least one second drive signal being applied substantially simultaneously,

wherein each of said first drive unit and said second drive unit are substantially similar in construction and comprise: a first [secondary] boost current mirror and a second [secondary] boost current mirror; each of said first and second [secondary] boost current mirrors being coupled to receive a boost signal; each respective [secondary] boost current mirror of said first and second [secondary] boost current mirrors responding to said control signals to present a [write] boost [current] signal level to said write head [in the same signal polarity as said representative logic level write drive signal presented by said respective current mirror].

Claim 16 (currently amended): A method for driving a write head in response to at least one data signal[;], the method comprising the steps of:

(a) in no particular order:

(1) providing a first drive unit coupled with said write head;

(2) providing a second drive unit coupled with said write head; and

(3) providing a control unit coupled with said first drive unit and said second drive unit; and

(b) operating said control unit to receive said at least one data signal and generate control signals to said first drive unit and said second drive unit in response to said at least one data signal; said control signals controlling said first drive unit to apply at least one first drive signal to a first write head connection locus of said write head in a first signal polarity and controlling said second drive unit to apply at least one second drive signal to a second write head connection locus of said write head in a second signal polarity opposite to said first signal polarity when said at least one data signal effects a signal excursion; said at least one first drive signal and said at least one second drive signal being substantially equal in magnitude; said at least one first drive

signal and said at least one second drive signal being applied substantially simultaneously,

wherein each of said first drive unit and said second drive unit are substantially similar in construction and comprise: a first logic level current mirror and a second logic level current mirror; each of said first and second logic level current mirrors being coupled to receive a direct current signal and responding to said control signals to present a [representative logic level write drive signal related to said] direct current signal level to said write head in one of said first signal polarity or said second signal polarity, and

wherein each of said first drive unit and said second drive unit comprise: a first [secondary] boost current mirror and a second [secondary] boost current mirror; each of said first and second [secondary] boost current mirrors being coupled to receive a boost signal; each respective [secondary] boost current mirror of said first and second [secondary] boost current mirrors responding to said control signals to present a [write] boost [current] signal level to said write head in the same signal polarity as said direct current signal level [representative logic level write drive signal presented by said respective current mirror].

2. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Dan I. Davidson whose telephone number is (571) 272-7552. The examiner can normally be reached on Monday-Friday.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Andrea L. Wellington, can be reached on (571) 272-4483. The fax phone number for the organization where this application or proceeding is assigned is (571) 273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

DID
Dan I Davidson
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SUPERVISORY PATENT EXAMINER